LZ2463A

1/4-type Color CCD Area Sensor with 470 k Pixels

DESCRIPTION

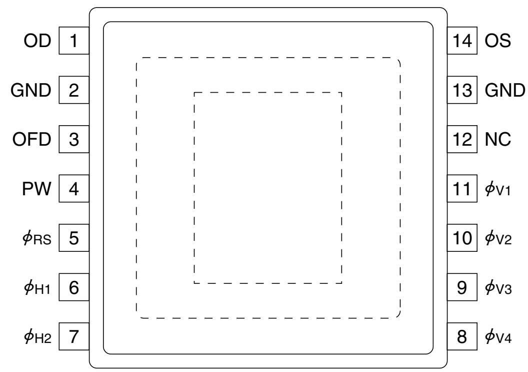
The LZ2463A is a 1/4-type (4.5 mm) solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices). With approximately 470 000 pixels (795 horizontal x 595 vertical), the sensor provides a stable high-resolution color image.

FEATURES

- Number of effective pixels : 752 (H) x 582 (V)
- Number of optical black pixels
  - Horizontal : 3 front and 40 rear
  - Vertical : 11 front and 2 rear
- Pixel pitch : 5.0 µm (H) x 4.7 µm (V)
- Mg, G, Cy, and Ye complementary color filters
- Low fixed-pattern noise and lag
- No burn-in and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Built-in overflow drain voltage circuit
- Horizontal shift register clock voltage : 3.6 V (TYP.)
- Variable electronic shutter (1/50 to 1/10 000 s)
- Compatible with PAL standard
- Package :
  14-pin half-pitch WDIP [Plastic]
  (WDIP014-P-0400A)
  Row space : 10.16 mm

PIN CONNECTIONS

14-PIN HALF-PITCH WDIP TOP VIEW



(WDIP014-P-0400A)

PRECAUTIONS

- The exit pupil position of lens should be more than 25 mm from the top surface of the CCD.
- Refer to **"PRECAUTIONS FOR CCD AREA SENSORS"** for details.

PIN DESCRIPTION

SYMBOL	PIN NAME
OD	Output transistor drain
OS	Output signals
ϕ_{RS}	Reset transistor clock
ϕ_{V1}, ϕ_{V2}, ϕ_{V3}, ϕ_{V4}	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
OFD	Overflow drain
PW	P-well
GND	Ground
NC	No connection

ABSOLUTE MAXIMUM RATINGS

(T_A = +25 ˚C)

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Output transistor drain voltage	V_{OD}	0 to +18	V	
Overflow drain voltage	V_{OFD}	Internal output	V	1
Reset gate clock voltage	$V_{\phi RS}$	–0.3 to +12	V	
Vertical shift register clock voltage	$V_{\phi V}$	–11.5 to +17.5	V	
Horizontal shift register clock voltage	$V_{\phi H}$	–0.3 to +12	V	
Voltage difference between P-well and vertical clock	V_{PW}-$V_{\phi V}$	–29 to 0	V	
Voltage difference between vertical clocks	$V_{\phi V}$-$V_{\phi V}$	0 to +15	V	2
Storage temperature	T_{STG}	–40 to +85	˚C	
Ambient operating temperature	T_{OPR}	–20 to +70	˚C	

NOTES :

1. Do not connect to DC voltage directly. When OFD is connected to GND, connect V_{OD} to GND. Overflow drain clock is applied below 27 Vp-p.
2. When clock width is below 10 µs, and clock duty factor is below 0.1%, voltage difference between vertical clocks will be below 28 V.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Ambient operating temperature		T_{OPR}		25.0		˚C	
Output transistor drain voltage		V_{OD}	14.55	15.0	15.45	V	
Overflow drain clock	p-p level	$V_{\phi OFD}$	22.5		24.5	V	1
Ground		GND		0.0		V	
P-well voltage		V_{PW}	–10.0		$V_{\phi VL}$	V	2
Vertical shift register clock	LOW level	$V_{\phi V1L}$, $V_{\phi V2L}$ $V_{\phi V3L}$, $V_{\phi V4L}$	–9.5	–9.0	–8.5	V	
	INTERMEDIATE level	$V_{\phi V1I}$, $V_{\phi V2I}$ $V_{\phi V3I}$, $V_{\phi V4I}$		0.0		V	
	HIGH level	$V_{\phi V1H}$, $V_{\phi V3H}$	14.55	15.0	15.45	V	
Horizontal shift register clock	LOW level	$V_{\phi H1L}$, $V_{\phi H2L}$	–0.05	0.0	0.05	V	
	HIGH level	$V_{\phi H1H}$, $V_{\phi H2H}$	3.3	3.6	5.5	V	
Reset gate clock	LOW level	$V_{\phi RSL}$	0.0		V_{OD} – 14.2	V	
	HIGH level	$V_{\phi RSH}$	V_{OD} – 9.7		10.0	V	
Vertical shift register clock frequency		$f_{\phi V1}$, $f_{\phi V2}$ $f_{\phi V3}$, $f_{\phi V4}$		15.63		kHz	
Horizontal shift register clock frequency		$f_{\phi H1}$, $f_{\phi H2}$		14.18		MHz	
Reset gate clock frequency		$f_{\phi RS}$		14.18		MHz	

NOTES :

- Connect NC to GND directly or through a capacitor larger than 0.047 μF.

1. Use the circuit parameter indicated in **"SYSTEM CONFIGURATION EXAMPLE"**, and do not connect to DC voltage directly.
2. V_{PW} is set below $V_{\phi VL}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

∗ To apply power, first connect GND and then turn on V_{OD}. After turning on V_{OD}, turn on PW first and then turn on other powers and pulses. Do not connect the device to or disconnect it from the plug socket while power is being applied.

CHARACTERISTICS (Drive method : Field accumulation)

(T_A = +25 ˚C, Operating conditions : The typical values specified in "**RECOMMENDED OPERATING CONDITIONS**". Color temperature of light source : 3 200 K, IR cut-off filter (CM-500, 1 mmt) is used.)

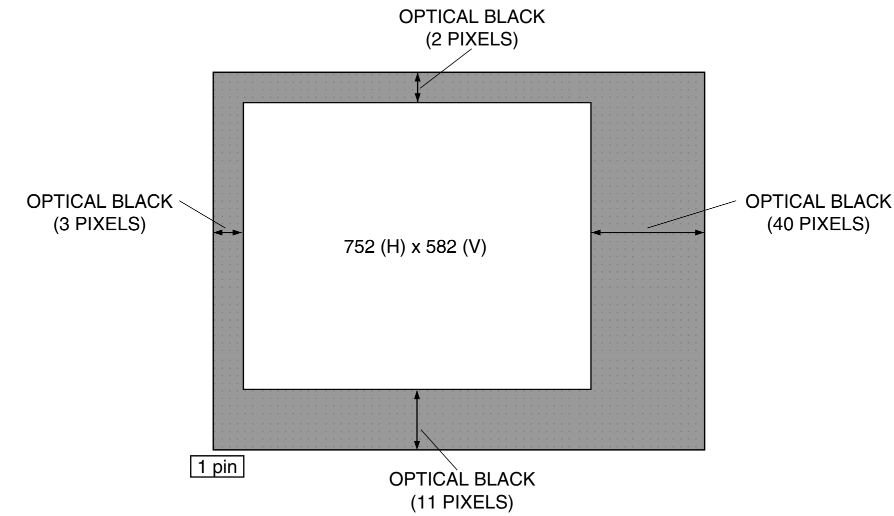
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	V_O		150		mV	2
Photo response non-uniformity	PRNU			15	%	3
Saturation output voltage	V_{SAT}	550	700		mV	4
Dark output voltage	V_{DARK}		0.5	3.0	mV	1, 5
Dark signal non-uniformity	DSNU		0.5	2.0	mV	1, 6
Sensitivity	R	150	210		mV	7
Smear ratio	SMR		–80	–70	dB	8
Image lag	AI			1.0	%	9
Blooming suppression ratio	ABL	1 000				10
Output transistor drain current	I_{OD}		4.0	8.0	mA	
Output impedance	R_O		350		Ω	
Vector breakup				7.0	˚, %	11
Line crawling				3.0	%	12
Luminance flicker				2.0	%	13

NOTES :

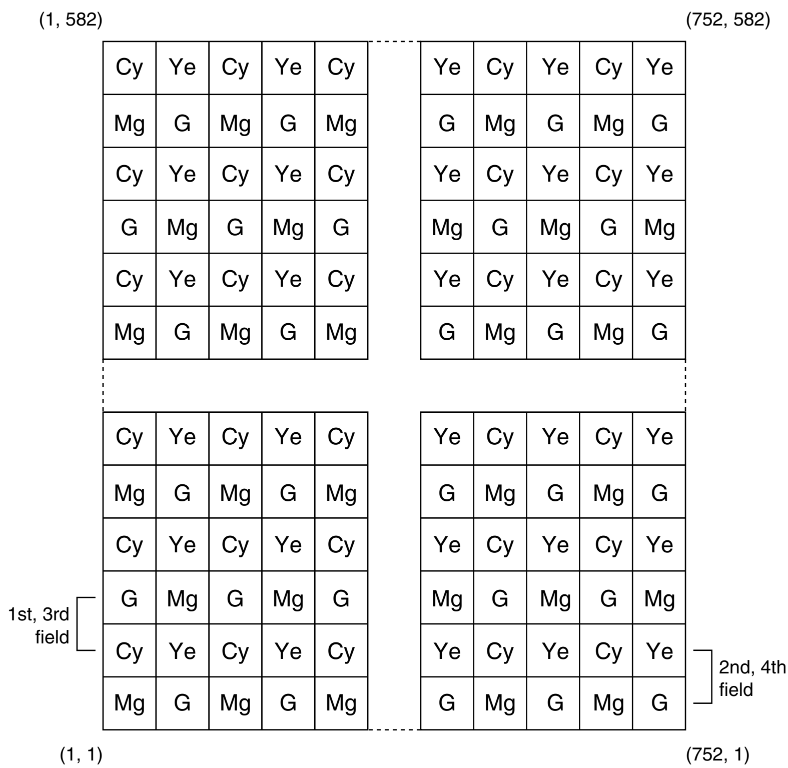
- Within the recommended operating conditions of V_{OD}, V_{OFD} of the internal output satisfies with ABL larger than 1 000 times exposure of the standard exposure conditions, and V_{SAT} larger than 550 mV.

1. T_A = +60 ˚C
2. The average output voltage under uniform illumination. The standard exposure conditions are defined as when Vo is 150 mV.
3. The image area is divided into 10 x 10 segments under the standard exposure conditions. Each segment's voltage is the average output voltage of all pixels within the segment. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and minimum values of each segment's voltage respectively.
4. The image area is divided into 10 x 10 segments. Each segment's voltage is the average output voltage of all pixels within the segment. V_{SAT} is the minimum segment's voltage under 10 times exposure of the standard exposure conditions.
5. The average output voltage under non-exposure conditions.
6. The image area is divided into 10 x 10 segments under non-exposure conditions. DSNU is defined by (Vdmax – Vdmin), where Vdmax and Vdmin are the maximum and minimum values of each segment's voltage respectively.
7. The average output voltage when a 1 000 lux light source with a 90% reflector is imaged by a lens of F4, f50 mm.
8. The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
9. The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
10. The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.
11. Observed with a vector scope when the color bar chart is imaged under the standard exposure conditions.
12. The difference between the average output voltage of the (Mg + Ye), (G + Cy) line and that of the (Mg + Cy), (G + Ye) line under the standard exposure conditions.
13. The difference between the average output voltage of the odd field and that of the even field under the standard exposure conditions.

PIXEL STRUCTURE



COLOR FILTER ARRAY

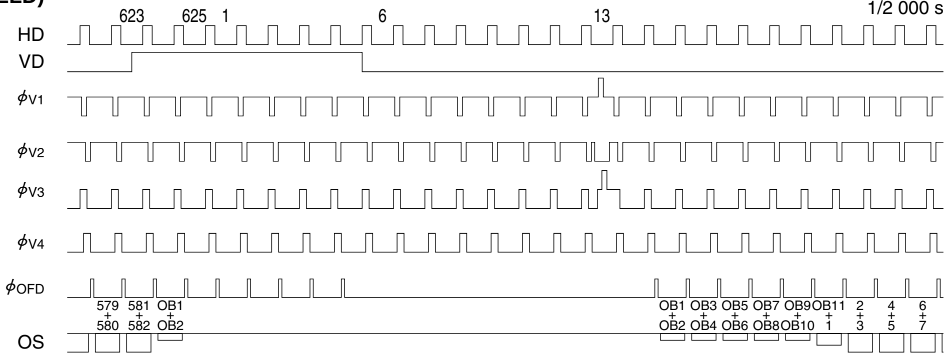


TIMING CHART

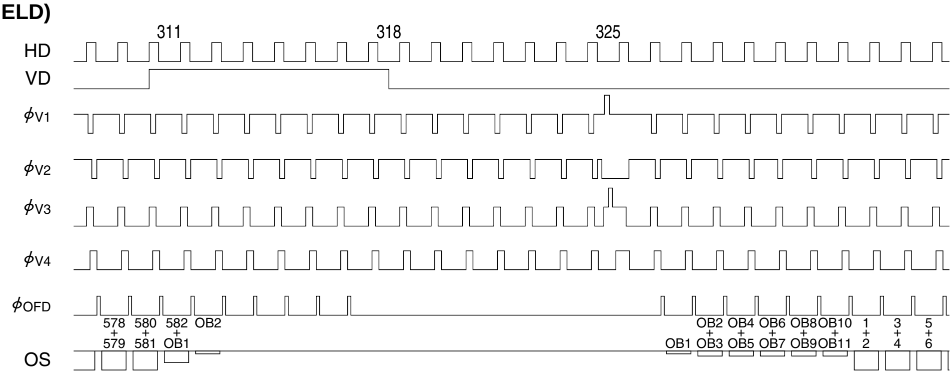
VERTICAL TRANSFER TIMING

Shutter speed
1/2 000 s

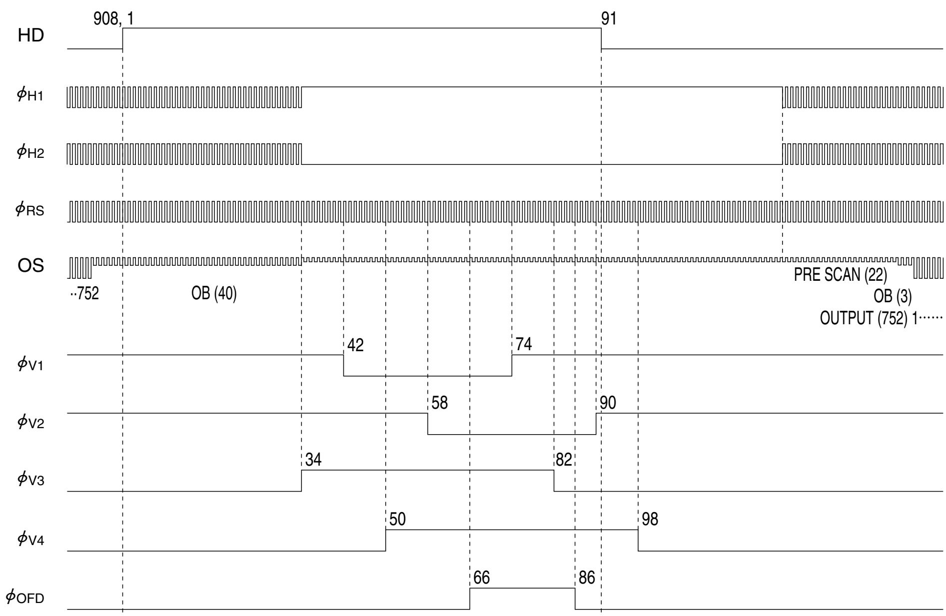
(1st, 3rd FIELD)



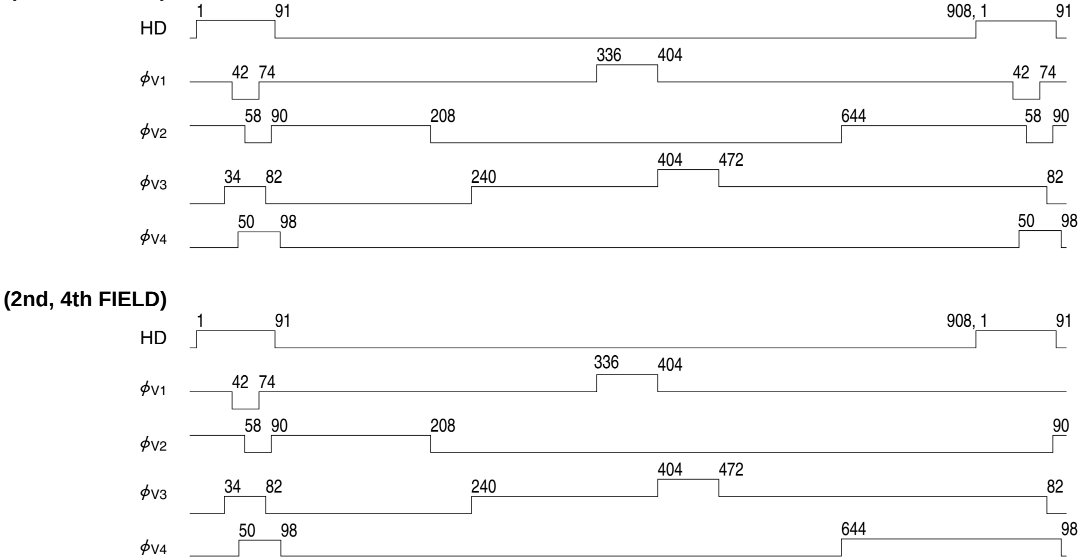
(2nd, 4th FIELD)



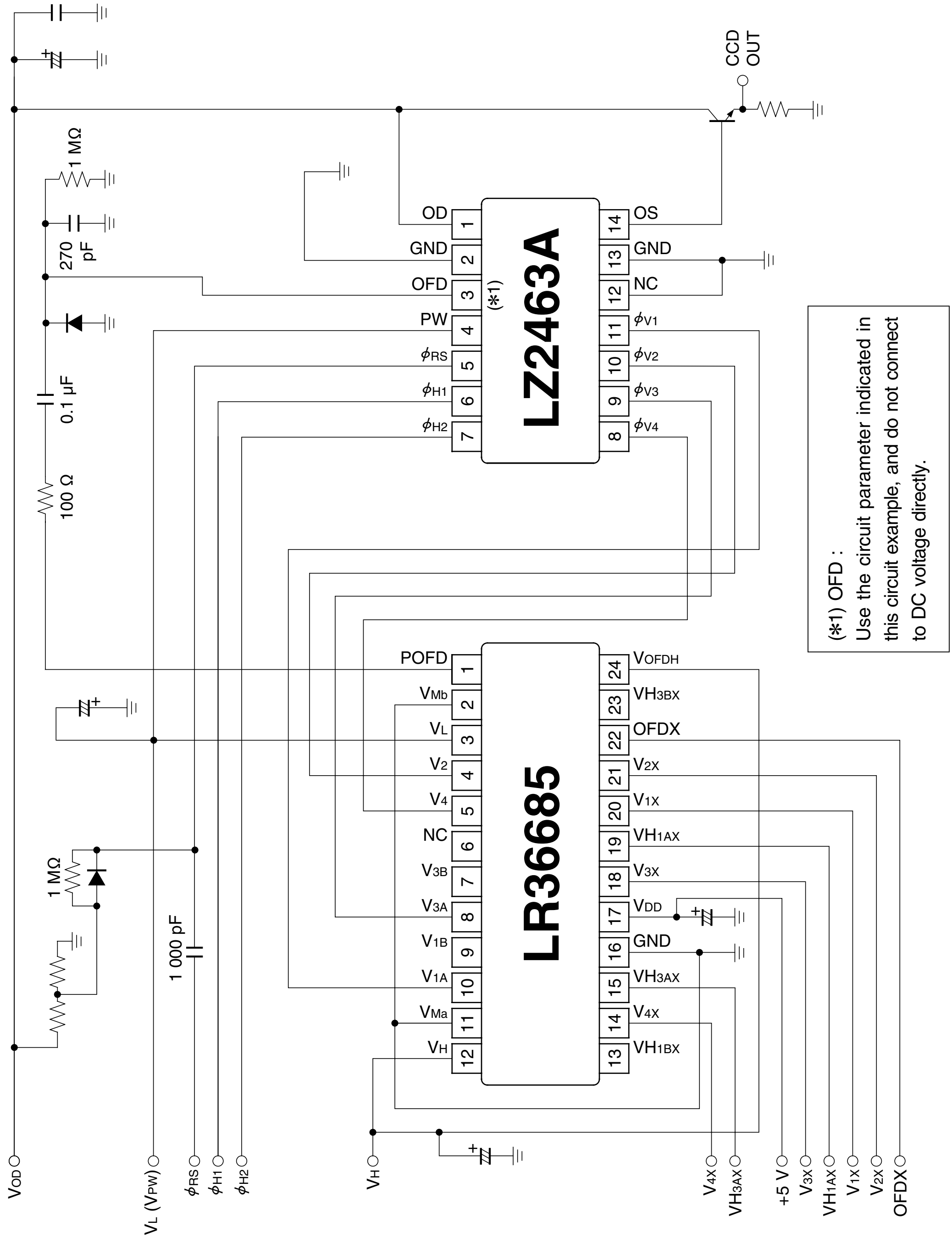
HORIZONTAL TRANSFER TIMING



READOUT TIMING



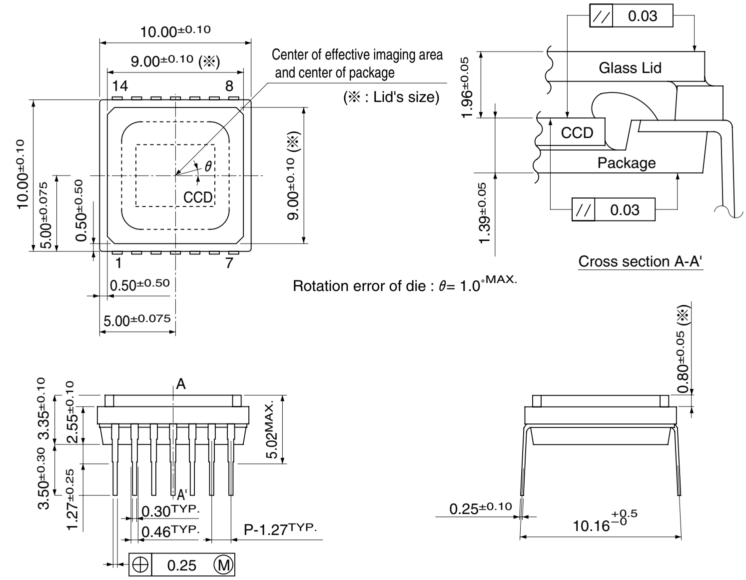
SYSTEM CONFIGURATION EXAMPLE



PACKAGE

(Unit : mm)

14 WDIP (WDIP014-P-0400A)



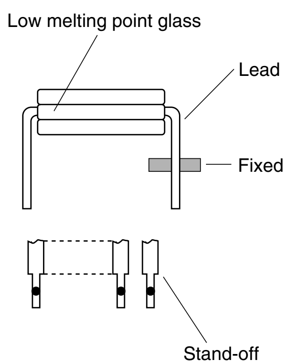
PRECAUTIONS FOR CCD AREA SENSORS

1. Package Breakage

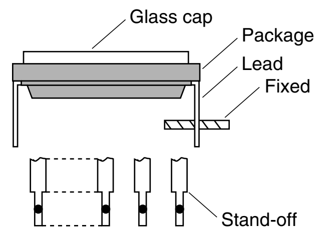
In order to prevent the package from being broken, observe the following instructions :

1) The CCD is a precise optical component and the package material is ceramic or plastic.
   Therefore,
   - Take care not to drop the device when mounting, handling, or transporting.
   - Avoid giving a shock to the package.
     Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.
2) When applying force for mounting the device or any other purposes, fix the leads between a joint and a stand-off, so that no stress will be given to the jointed part of the lead. In addition, when applying force, do it at a point below the stand-off part.

   (In the case of ceramic packages)
   – The leads of the package are fixed with low melting point glass, so stress added to a lead could cause a crack in the low melting point glass in the jointed part of the lead.



   (In the case of plastic packages)
   – The leads of the package are fixed with package body (plastic), so stress added to a lead could cause a crack in the package body (plastic) in the jointed part of the lead.



3) When mounting the package on the housing, be sure that the package is not bent.
   – If a bent package is forced into place between a hard plate or the like, the package may be broken.
4) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
   Therefore,
   - Do not hit the glass cap.
   - Do not give a shock large enough to cause distortion.
   - Do not scrub or scratch the glass surface.
   – Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.

2. Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD. Therefore, take the following anti-static measures when handling the CCD :

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.

3) To avoid generating static electricity,
   a. do not scrub the glass surface with cloth or plastic.
   b. do not attach any tape or labels.
   c. do not clean the glass surface with dust-cleaning tape.
4) When storing or transporting the device, put it in a container of conductive material.

3. Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions :

1) Handle the CCD in a clean environment such as a cleaned booth. (The cleanliness level should be, if possible, class 1 000 at least.)
2) Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended :
   - Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
   - The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.
   – Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note : In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommended that the above procedures should be taken to wipe out dust and contamination before using the device.

4. Other

1) Soldering should be manually performed within 5 seconds at 350 °C maximum at soldering iron.
2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.
3) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.